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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,506	06/28/2001	Jin Murayama	107317-00032	4994

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EXAMINER	
VIEAUX, GARY	
ART UNIT	**PAPER NUMBER**
2622	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,506	MURAYAMA ET AL.	
	Examiner	Art Unit	
	Gary C. Vieaux	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, and 3-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

The Amendment filed May 24, 2006 has been received and made of record. In response to the Office Action dated February 24, 2006, claims 1 and 8 have been amended. Claim 2 has been previously cancelled. Claims 1 and 3-17 are currently pending.

Response to Arguments

Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5, 8-12, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA), in view of Miwada (US 5,220,210), in view of Hatta (US 5,087,964), in view of Masuda et al. (US 5,249,055), in view of Ishii et al. (US 6,022,792), in view of Examiner's Official Notice.

Regarding claim 1, Applicant, in the Background of the Invention, discloses a linear image sensor chip comprising a semiconductor substrate having an elongated shape (p. 1 line 20), an image pickup section formed on said semiconductor substrate (p. 1 lines 20-21), said image pickup section including (i) at least one photodiode group composed of a plurality of photodiodes formed in one surface of said semiconductor substrate along a longitudinal direction of said semiconductor substrate (p. 2 lines 7-9) and (ii) a charge transfer element provided for each said photodiode group (p. 1 lines 23-24), a peripheral circuit section (p. 3 lines 3-5), a plurality of bonding pads formed on the surface of said semiconductor substrate in the opposite end areas along the longitudinal direction, which is the alternative option to being formed in a central area of the semiconductor substrate (p. 3 lines 6-9), each of said bonding pads having an exposed surface for external connection (p. 3 lines 10-11), a light-suppressing layer formed above said semiconductor substrate and covering a peripheral area (p.3 lines 16-17), and bonding wires connecting the bonding pads with lead electrodes (p.3 lines 18-21.)

The Applicant Admitted Prior Art (AAPA) is not found to explicitly disclose the photodiodes being formed only in a central area of a surface of the semiconductor substrate along a longitudinal direction, the light-suppressing layer covering a peripheral area of each said photodiode, the peripheral circuit section being formed in a peripheral area of the surface of said semiconductor substrate and being external to said central area in the longitudinal direction of the semiconductor substrate, or the bonding pads having an exposed central surface area, or a plurality of metal lines formed on the

surface of said semiconductor substrate, each of said metal lines having an end connected to one of said bonding pad and another end connected to said peripheral circuit or said charge transfer element, or a passivation layer formed to cover an outer surface area of each of said bonding pads.

Nevertheless, Miwada teaches photodiodes being formed only in a central area of a surface of the semiconductor substrate along a longitudinal direction (fig. 2.) It would have been obvious to one of ordinary skill in the art at the time of the invention to employ photodiodes formed only in a central area of a surface of the semiconductor substrate along a longitudinal direction as taught by Miwada, with the image sensor as taught by the AAPA, in order to minimize empty area on a linear image sensor chip.

Hatta teaches a light-suppressing layer which only allows light to pass through to an image area (fig. 16 and 17 indicator 7; col. 1 lines 24-33.) It would have been obvious to one of ordinary skill in the art at the time of the invention to include the light-suppressing layer to cover everywhere but where the light strikes the image area as taught by Hatta, with photodiodes of the image sensor as taught by Miwada and the AAPA, in order to ensure the only light intended to strike the photodiode reaches the photodiode, as well as to prevent light from radiating to a part other than the imaging area.

Further, it is well known in the art to provide a peripheral circuit section formed in a peripheral area of said surface of said semiconductor substrate, said peripheral area being external to said central area in the longitudinal direction as demonstrated by Masuda (figs. 10 and 4a indicator 7.) It would have been obvious to one of ordinary skill

in the art at the time of the invention to include circuitry peripheral to the photodiodes (figs. 10 and 4a indicator 4) and the charge transfer elements (figs. 10 and 4a indicator 5) as taught by Masuda, with the image sensor as taught by Hatta, Miwada, and the AAPA in order to minimize the width of the image sensor chip, resulting in a more compact image sensor, which is particularly important in full-page-width imaging.

Additionally, Ishii is found to teach both bonding pads having an exposed central surface area (fig. 2 indicator 9) and a passivation layer formed to cover an outer surface area of each of said bonding pads (fig. 2 indicator 10, col. 2 lines 10-13.) It would have been obvious to one of ordinary skill in the art at the time of the invention to provide for an exposed central surface area of the bonding pads, as well to cover an outer surface area of each of said bonding pads with a passivation layer as taught by Ishii, with the the image sensor as taught by Masuda, Hatta, Miwada, and the AAPA, in order to allow for connection of the bonding wires to the bonding pad and for insulation of the substrate components, respectively.

Official Notice was taken regarding the etching of metal lines on a semiconductor substrate for the purposes of forming bonding pads, interconnects and trace runs; a practice that is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention for the image sensor as taught by Ishii, Masuda, Hatta, Miwada, and the AAPA, to include a plurality of metal lines formed on the surface of said semiconductor substrate, each of said metal lines having an end connected to one of said bonding pad and another end connected to the circuitry peripheral to the photodiodes in order to be able to pass signal from the photodiodes to

the bonding pads and eventually to circuitry external to the semiconductor substrate for additional processing, such as to a printing apparatus, an image memory or an image display device.

It is noted by the Examiner that applicant has failed to specifically traverse the old and well known statement above, and therefor the etching of metal lines on a semiconductor substrate for the purposes of forming bonding pads, interconnects and trace runs is hereafter taken to be admitted prior art. See MPEP § 2144.03(c).

Regarding claim 3, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 3 (see the 103(a) rejection to claim 1 supra) including teaching an image sensor chip wherein each of said bonding pads is disposed outer than said peripheral circuit section with respect to the longitudinal direction ('210 – figs. 1 and 2 indicators a_n; col. 2 line 65 – col. 3 line 2.)

Regarding claim 4, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 4 (see the 103(a) rejection to claim 1 supra) including teaching an image sensor chip wherein said light-suppressing layer covers also said peripheral circuit section (figs. 1-3 indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents light from radiating to a part other than the imaging area.)

Regarding claim 5, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 5 (see the 103(a) rejection to claim 1 supra) including teaching an image sensor chip wherein said light-suppressing layer covers said metal lines at least in a region sideward along said at least one photodiode

group (figs. 1-3 indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents light from radiating to a part other than the imaging area.)

Regarding claim 8, Applicant, in the Background of the Invention, discloses a linear image sensor comprising a package including a bottom portion, sidewall portions and a lid portion (p. 3 lines 13-17), and a plurality of lead electrodes, passing through said sidewall portions, and reaching an external space (p. 3 lines 18-19), said bottom portion and said sidewall portions being made of light shielding material (p.3 lines 14-15) and said lid portion having a window made of transparent material (p. 3 line 15), a linear image sensor chip fixed in the inner space of said package (p. 3 line 13), said linear image sensor chip including (1) a semiconductor substrate (p. 1 line 20) having an elongated shape along a direction generally coincident with the longitudinal direction (p.2 lines 7-9), (2) an image pickup section formed on said semiconductor substrate, said image pickup section including (i) at least one photodiode group composed of a plurality of photodiodes formed in one surface of said semiconductor substrate along a longitudinal direction of said semiconductor substrate (p. 2 lines 7-9) and (ii) a charge transfer element provided for each said photodiode group (p. 1 line 23-24), (3) a peripheral circuit section (p. 3 line 3-5), (4) a plurality of bonding pads formed on the surface of said semiconductor substrate in the opposite end areas along the longitudinal direction, which is the alternative option to being formed in a central area of the semiconductor substrate (p. 3 lines 6-9), each of said bonding pads having an exposed surface for external connection (p. 3 lines 10-11), a light-suppressing layer formed above said semiconductor substrate and covering a peripheral area (p.3 lines 16-17),

and a plurality of bonding wires each electrically connecting one of said lead electrodes to a predetermined one of said bonding pads (p. 3 lines 18-21.)

The AAPA is not found to explicitly disclose the photodiodes being formed only in a central area of a surface of the semiconductor substrate along a longitudinal direction, a package defining an elongated inner space, the lead electrodes extending from an end region of the elongated inner space, the lid portion having an elongated window, the semiconductor substrate being generally coincident with the longitudinal direction of said bottom portion, the peripheral circuit section being formed in a peripheral area of the surface of said semiconductor substrate and being external to said central area in the longitudinal direction of the semiconductor substrate,, each of the bonding pads having an exposed central surface area, a plurality of metal lines formed on the surface of the semiconductor substrate, each of the metal lines having an end connected to one of the bonding pads and another end connected to the peripheral circuit or the charge transfer element, and a light-suppressing layer formed above the semiconductor substrate and covering a peripheral area of each said photodiode, or a passivation layer formed to cover an outer surface area of each of said bonding pads.

Nevertheless, Miwada teaches photodiodes being formed only in a central area of a surface of the semiconductor substrate along a longitudinal direction (fig. 2.) It would have been obvious to one of ordinary skill in the art at the time of the invention to employ photodiodes formed only in a central area of a surface of the semiconductor substrate along a longitudinal direction as taught by Miwada, with the image sensor as taught by the AAPA, in order to minimize empty area on a linear image sensor chip.

Hatta is found to teach a package defining an elongated inner space (fig. 3), the lid portion having an elongated window (fig. 3 indicator 22), and a semiconductor substrate (fig. 3 indicator 14) being generally coincident with the longitudinal direction of the package (fig. 3.) It would have been obvious to one of ordinary skill in the art at the time of the invention to construct a package as taught by Hatta, with the image sensor as taught by Miwada and the AAPA, so that the elongated semiconductor substrate of the line image sensor taught by the AAPA would be accommodated within the package.

Hatta further teaches the lead electrodes extending from an end region of the elongated inner space (fig. 16 indicators 5 and 6.) It would have been obvious to one of ordinary skill in the art at the time of the invention to located the lead electrodes at the end regions as taught by Hatta, in order to coincide with the bonding pads, which are located outer than the photodiode group with respect to the longitudinal direction of the semiconductor substrate of the image sensor as taught by Miwada and the AAPA, and therefore requiring the less wiring due to a shorter distance, as well as potentially less chance of requiring wires to cross.

Hatta also teaches a light-suppressing layer which only allows light to pass through to an image area (fig. 1 and 2 indicator 7; col. 1 lines 24-33.) It would have been obvious to one of ordinary skill in the art at the time of the invention to include the light-suppressing layer to cover everywhere but where the light strikes the image area as taught by Hatta, with photodiodes of the image sensor as taught by Miwada and the AAPA, in order to ensure the only light intended to strike the photodiode reaches the

photodiode, as well as to prevent light from radiating to a part other than the imaging area.

Further, it is well known in the art to provide a peripheral circuit section formed in a peripheral area of said surface of said semiconductor substrate, said peripheral area being external to said central area in the longitudinal direction as demonstrated by Masuda (figs. 10 and 4a indicator 7.) It would have been obvious to one of ordinary skill in the art at the time of the invention to include circuitry peripheral to the photodiodes (figs. 10 and 4a indicator 4) and the charge transfer elements (figs. 10 and 4a indicator 5) as taught by Masuda, with the image sensor as taught by Hatta, Miwada, and the AAPA in order to minimize the width of the image sensor chip, resulting in a more compact image sensor, which is particularly important in full-page-width imaging.

Additionally, Ishii is found to teach both bonding pads having an exposed central surface area (fig. 2 indicator 9) and a passivation layer formed to cover an outer surface area of each of said bonding pads (fig. 2 indicator 10, col. 2 lines 10-13.) It would have been obvious to one of ordinary skill in the art at the time of the invention to provide for an exposed central surface area of the bonding pads, as well to cover an outer surface area of each of said bonding pads with a passivation layer as taught by Ishii, with the image sensor as taught by Masuda, Hatta, Miwada, and the AAPA, in order to allow for connection of the bonding wires to the bonding pad and for insulation of the substrate components, respectively.

Official Notice is taken regarding the etching of metal lines on a semiconductor substrate for the purposes of forming bonding pads, interconnects and trace runs; a

practice that is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention for the image sensor as taught by Ishii, Masuda, Hatta, Miwada, and the AAPA to include a plurality of metal lines formed on the surface of said semiconductor substrate, each of said metal lines having an end connected to one of said bonding pad and another end connected to the circuitry peripheral to the photodiodes in order to be able to pass signal from the photodiodes to the bonding pads and eventually to circuitry external to the semiconductor substrate for additional processing, such as to a printing apparatus, an image memory or an image display device.

It is noted by the Examiner that applicant has failed to specifically traverse the old and well known statement above, and therefor the etching of metal lines on a semiconductor substrate for the purposes of forming bonding pads, interconnects and trace runs is hereafter taken to be admitted prior art. See MPEP § 2144.03(c).

Regarding claim 9, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 9 (see the 103(a) rejection to claim 8 supra) including teaching an image sensor wherein all the bonding pads having exposed surfaces are formed on the surface of said semiconductor substrate outer than said at least one photodiode group with respect to the longitudinal direction of said semiconductor substrate ('210 – figs. 1 and 2 indicators a_n; col. 2 line 65 – col. 3 line 2.)

Regarding claim 10, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 10 (see the 103(a) rejection to claim 8 supra) including teaching an image sensor wherein each of said bonding pads is

disposed outer than said peripheral circuit section with respect to the longitudinal direction of said semiconductor substrate ('210 – figs. 1 and 2 indicators a_n; col. 2 line 65 – col. 3 line 2.)

Regarding claim 11, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 11 (see the 103(a) rejection to claim 8 supra) including teaching an image sensor wherein said light-suppressing layer covers also said peripheral circuit section (figs. 1-3 indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents light from radiating to a part other than the imaging area.)

Regarding claim 12, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 12 (see the 103(a) rejection to claim 8 supra) including teaching an image sensor wherein said light-suppressing layer covers said metal lines at least in a region sideward along said at least one photodiode group (figs. 1-3 indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents light from radiating to a part other than the imaging area.)

Regarding claim 15, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 15 (see the 103(a) rejection to claim 8 supra) including teaching an image sensor wherein each said lead electrode is disposed outer than said image pickup section with respect to the longitudinal direction of said semiconductor substrate ('210 – fig. 1 indicators 3-n.)

Regarding claim 16, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 16 (see the 103(a) rejection to claim 8

supra) including teaching an image sensor wherein each said lead electrode is disposed outer than said peripheral circuit section with respect to the longitudinal direction of said semiconductor substrate ('210 – fig. 1, indicators 3, 2 and 10, respectively.) It is also noted that Masuda is found to disclose the peripheral circuit section outer than the image pickup section with respect to the longitudinal direction (figs. 10 and 4a indicator 7), includes both the image pickup section and the peripheral circuit section on the same semiconductor substrate (fig. 10 indicator 3; col. 1 lines 27-39.)

Regarding claim 17, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 5 (see the 103(a) rejection to claim 1 supra) including teaching an image sensor chip wherein said light-suppressing layer covers said metal lines at least in a region sideward along said at least one photodiode group (figs. 1-3 indicator 17; figs. 16 and 17 indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents light from radiating to a part other than the imaging area) and an edge portion of each of said bonding pads (figs. 1-3 indicators 15 and 17; figs. 16 and 17 indicators 4 and 7.)

Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA), in view of Miwada (US 5,220,210), in view of Hatta (US 5,087,964), in view of Masuda et al. (US 5,249,055), in view of Ishii et al. (US 6,022,792), in view of Examiner's Official Notice, in further view of Kawai et al. (US 6,078,685), in further view of Phillips et al. (5,773,814.)

Regarding claim 6, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 6 (see the 103(a) rejection to claim 1 supra) except for teaching an image sensor chip wherein said image pickup section includes four photodiode groups juxtaposed along a direction crossing the longitudinal direction, said peripheral circuit section includes an output amplifier provided for each said charge transfer element and electrically connected to an output terminal of a corresponding charge transfer element, and the linear image sensor chip further comprises a color filter array disposed for each of three photodiode groups of said four photodiode groups, said color filter arrays generally constituting a multicolor color filter array necessary for taking a color image.

Nevertheless, Kawai is found to teach a plurality of light receiving units having a plurality of color filters, which include peripheral circuit sections that include output amplifiers for each charge transfer element and are electrically connected to an output terminal of the corresponding charge transfer element (figs. 2 and 3; col. 1 line 33 – col. 2 line16.) It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kawai, with the linear image sensor chip as taught by the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice, in order to capture color images, while still attempting to minimize the width of the image sensor chip through placement of the peripheral circuit components.

Further, Phillips teaches an image sensor in which the image pickup section includes four sensor array groups juxtaposed along a direction crossing the longitudinal direction (fig. 6A and fig. 1 indicator 118), which also includes color filters disposed for

three of the four sensor array groups, with the color filters generally constituting the multicolor color filter configuration necessary for taking a color image, and the fourth sensor array group not having a filter so that black and white or grayscale image capture can be performed (fig. 6A; col. 7 lines 7-38.) It would have been further obvious to one of ordinary skill in the art at the time of the invention to incorporate the four sensor array groups, with three of the four groups having color filters combinations necessary for taking a color image as taught by Phillips, with the linear image sensor chip as taught by the AAPA, Miwada, Hatta, Masuda, Ishii, Examiner's Official Notice and Kawai, so that the linear image sensor chip can be employed for black and white or grayscale image capture, in addition to the capture of color images.

Regarding claim 13, the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice teach all the limitations of claim 13 (see the 103(a) rejection to claim 8 supra) except for teaching an image sensor wherein said image pickup section includes four photodiode groups juxtaposed along a direction crossing the longitudinal direction of said semiconductor substrate, said peripheral circuit section includes an output amplifier provided for each said charge transfer element and electrically connected to an output terminal of a corresponding charge transfer element, and said linear image sensor chip further comprises a color filter array disposed for each of three photodiode groups of said four photodiode groups, said color filter arrays generally constituting a multicolor color filter array necessary for taking a color image.

Nevertheless, Kawai is found to teach a plurality of light receiving units having a plurality of color filters, which include peripheral circuit sections that include output

amplifiers for each charge transfer element and are electrically connected to an output terminal of the corresponding charge transfer element (figs. 2 and 3; col. 1 line 33 – col. 2 line16.) It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kawai, with the linear image sensor as taught by the AAPA, Miwada, Hatta, Masuda, Ishii, and Examiner's Official Notice, in order to capture color images, while still attempting to minimize the width of the image sensor through placement of the peripheral circuit components.

Further, Phillips teaches an image sensor in which the image pickup section includes four sensor array groups juxtaposed along a direction crossing the longitudinal direction (fig. 6A and fig. 1 indicator 118), which also includes color filters disposed for three of the four sensor array groups, with the color filters generally constituting the multicolor color filter configuration necessary for taking a color image, and the fourth sensor array group not having a filter so that black and white or grayscale image capture can be performed (fig. 6A; col. 7 lines 7-38.) It would have been further obvious to one of ordinary skill in the art at the time of the invention to incorporate the four sensor array groups, with three of the four groups having color filters combinations necessary for taking a color image as taught by Phillips, with the linear image sensor as taught by the AAPA, Miwada, Hatta, Masuda, Ishii, Examiner's Official Notice and Kawai, so that the linear image sensor chip can be employed for black and white or grayscale image capture, in addition to the capture of color images.

Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA), in view of Miwada (US 5,220,210), in view of Hatta (US 5,087,964), in view of Masuda et al. (US 5,249,055), in view of Ishii et al. (US 6,022,792), in view of Examiner's Official Notice, in view of Kawai et al. (US 6,078,685), in view of Phillips et al. (5,773,814), in further view of Sakamoto et al. (US 5,648,653.)

Regarding claim 7, the AAPA, Miwada, Hatta, Masuda, Ishii, Examiner's Official Notice, Kawai and Phillips teach all the limitations of claim 7 (see the 103(a) rejection to claim 6 supra) except for teaching an image sensor chip further comprising a color filter array disposed above remaining one of said four photodiode groups.

Nevertheless, Sakamoto teaches employing four color filters disposed above four image sensors groups, with the fourth filter converting infrared (figs. 1 and 2; col. 3 line 46 – col. 4 line 39.) It would have been obvious to one of ordinary skill in the art at the time of the invention to arrange four color filters above four image sensors groups as taught by Sakamoto, with the image sensor chip as taught by the AAPA, Miwada, Hatta, Masuda, Ishii, Examiner's Official Notice, Kawai and Phillips, so that the linear image sensor chip can be employed for color or black and white or grayscale image capture, in addition to the capture of images in the visible and invisible regions.

Regarding claim 14, the AAPA, Miwada, Hatta, Masuda, Ishii, Examiner's Official Notice, Kawai and Phillips teach all the limitations of claim 14 (see the 103(a) rejection to claim 13 supra) except for teaching an image sensor further comprising a color filter array disposed above remaining one of said four photodiode groups.

Nevertheless, Sakamoto teaches employing four color filters disposed above four image sensors groups, with the fourth filter converting infrared (figs. 1 and 2; col. 3 line 46 – col. 4 line 39.) It would have been obvious to one of ordinary skill in the art at the time of the invention to arrange four color filters above four image sensors groups as taught by Sakamoto, with the image sensor as taught by the AAPA, Miwada, Hatta, Masuda, Ishii, Examiner's Official Notice, Kawai and Phillips, so that the linear image sensor chip can be employed for color or black and white or grayscale image capture, in addition to the capture of images in the visible and invisible regions.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

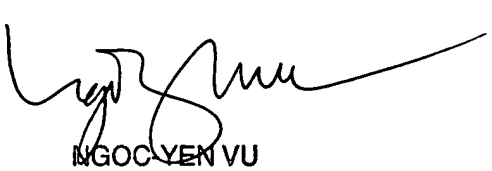
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary C. Vieaux whose telephone number is 571-272-7318. The examiner can normally be reached on Monday - Friday, 8:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen T. Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gary C. Vieaux
Examiner
Art Unit 2622

Gcv2



NGOC YEN VU
SUPERVISORY PATENT EXAMINER